

- 1 1. A system comprising:
 - 2 an execution pipeline;
 - 3 a power delivery unit to provide power to the execution pipeline at a specified
 - 4 operating point;
 - 5 a digital throttle to estimate a power state, responsive to activity of the execution
 - 6 pipeline and the specified operating state, and to trigger a change in the operating state,
 - 7 responsive to the estimated power state reaching a first threshold.
- 1 2. The system of claim 1, wherein the power delivery unit includes a clock gating circuit to
- 2 control power delivery to one or more units of the execution pipeline.
- 1 3. The system of claim 2, wherein the digital throttle comprises an activity monitor to
- 2 estimate an activity level responsive to a signal from the clock gating circuit, the activity monitor
- 3 including a scaling unit to adjust the estimated activity level, responsive to the current operating
- 4 point.
- 1 4. The system of claim 3, wherein the scaling unit includes:
 - 2 a look-up table to store scaling factors for a plurality of operating points; and
 - 3 a multiplier to multiply the estimated activity level by the scaling factor
 - 4 associated with the current operating point.

The system of claim 3, wherein the monitor unit further comprises:

a plurality of weight units, each weight unit being associated with one of the units of the execution pipeline; and

an adder to receive a first or second value from each weight unit, responsive to the signal from the clock gating circuit.

An apparatus comprising:

an execution pipeline including one or more units to execute an instruction at a current operating point;

a gate unit to indicate an activity state for the one or more units;

an activity monitor to estimate an activity level for the processor, responsive to the gate unit and the current operating point; and

a throttle circuit to adjust the operating point, responsive to a power state determined from the estimated activity level reaching a first threshold.

The system of claim 1, wherein the activity monitor includes:

a look-up table to store scaling factors corresponding to a plurality of operating points; and

4 a scaling unit to adjust the activity level according to a scaling factor appropriate
5 for the specified operating point.

1 8. The system of claim 7, further comprising a conversion circuit to determine a power state
2 from the adjusted activity level.

1 9. The system of claim 8, wherein the conversion circuit compares the adjusted activity
2 level with a threshold level and stores the difference in an accumulator.

1 10. The system of claim 9, wherein the conversion unit scales the threshold level responsive
2 to the current operating point.

1 11. A processor comprising:
2 an execution pipeline;
3 a clock gating circuit to control power delivery to one or more units of the
4 execution pipeline;
5 a monitor unit to estimate an activity level of the execution pipeline, responsive to
6 a status signal from the clock gating circuit;
7 a scaling unit to adjust the estimated activity level, responsive to an operating
8 point of the processor; and

9 a threshold comparator to determine if the scaled, estimated activity level meets a
10 first threshold level.

1 12. The processor of claim 11, wherein the scaling unit includes a look-up table and a
2 multiplier, the look-up table to provide a scale factor to the multiplier, responsive to the
3 operating point of the processor.

1 13. The processor of claim 12, wherein the operating point of the processor is specified by a
2 voltage and a frequency.

1 14. The processor of claim 11, further comprising an accumulator to increment a stored value
2 by a difference between the scaled, estimated activity and the first threshold if the scaled activity
3 exceeds the first threshold.

1 15. The processor of claim 14, further comprising a comparator to compare the stored value
2 with a second threshold and to assert a power-reduction signal if the stored value reaches the
3 second threshold value.

1 16. The processor of claim 11, wherein the activity monitor includes an adder having one or
2 more weighted inputs, each input associated with the one or more pipeline units, respectively.

1 17. The processor of claim 16, wherein the status signal comprises one or more status signals
2 associated with the one or more pipeline units, respectively.

18. The processor of claim 17, wherein the adder sums a first or a second value from each of
the weighted inputs, responsive to a state of the associated status signal

1 19. A method for controlling power consumption in a processor comprising:
2 monitoring activity states for pipeline units of the processor;
3 estimating a power state for the processor using the monitored activity states and
4 an operating point of the processor;
5 comparing the estimated power state with a threshold value; and
6 adjusting the operating point of the processor if the estimated power state exceeds
7 the threshold value.

1 20. The method of claim 19, wherein estimating the power state comprises:
2 determining an activity level from the monitored activity states;
3 scaling the activity level according to the operating point;
4 normalizing the scaled activity level relative to a first threshold; and
5 accumulating the normalized, scaled activity level for a series of clock intervals.

1 21. The method of claim 19, wherein monitoring activity states comprises monitoring status
2 signals provided by gate units associated with the pipeline units of the processor.

1 22. The method of claim 19, wherein each gate unit controls a clock signal to activate its
2 associated pipeline unit as it is needed.

1 23. The method of claim 22, wherein adjusting the operating point of the processor comprises
2 adjusting a frequency of the clock signal.

1 24. The method of claim 23, wherein adjusting the operating point further comprises
2 adjusting a voltage of the clock signal.

1 25. The method of claim 19, wherein estimating the activity level comprises:
2 adding a first or a second weight value to a sum, responsive to a pipeline unit
3 being in a first or a second activity state, respectively; and
4 scaling the sum by a factor associated with the current operating point.

1 26. The method of claim 25, wherein estimating the activity level further comprising adding
2 a weight to the sum to represent pipeline units that operate in a single activity state.

1 27. A computer system comprising:
2 a memory system to store instructions for execution;
3 an instruction execution pipeline including a plurality of units to execute the
4 instructions;
5 a power deliver system to deliver power to the execution pipeline at a current
6 operating point;
7 an activity monitor to estimate an activity level for the execution pipeline at the
8 current operating point; and
9 a throttle circuit to adjust the current operating point, responsive to a power state
10 determined from the activity level falling outside a specified range.

1 28. The computer system of claim 27, wherein the power delivery system includes plural gate
2 units, each gate unit to indicate a first or second activity state for a unit of the execution pipeline,
3 according to the unit's being activate or inactive in a clock interval.

1 29. The computer system of claim 28, wherein activity monitor includes an adder to add a
2 first or a second weight to the activity level, responsive to the gate unit indicating a first or
3 second state for its associated pipeline unit in the clock interval.

1 30. The system of claim 29, wherein the activity monitor further includes a scale unit to scale
2 the activity level for the clock interval according to the current operating point of the processor.